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(54) Abstract Title
Active pixel sensor with electronic shutter

(57) An active pixel sensor with an electronic shutter is capable of obtaining an auto exposure function so that all pixels have the identical photosensitive time to enable a uniform brightness across a display screen. Means such as a diode D1 for generating a photo-electric charge in accordance with light incident thereon is connected to means M2 for amplifying the charge and means M3 for outputting the charge in response to a selection signal. Switching means M4 passes the charge for a predetermined time in accordance with an externally inputted shutter control signal to means M5 for storing the charge for a predetermined time. The charge from the storage means M5 is supplied to the amplifying means M2, and the storage means is reset in accordance with an electric charge resetting signal. The charge on the diode D1 may be reset at the same time by a signal to a transistor in series with it.

FIG. 2

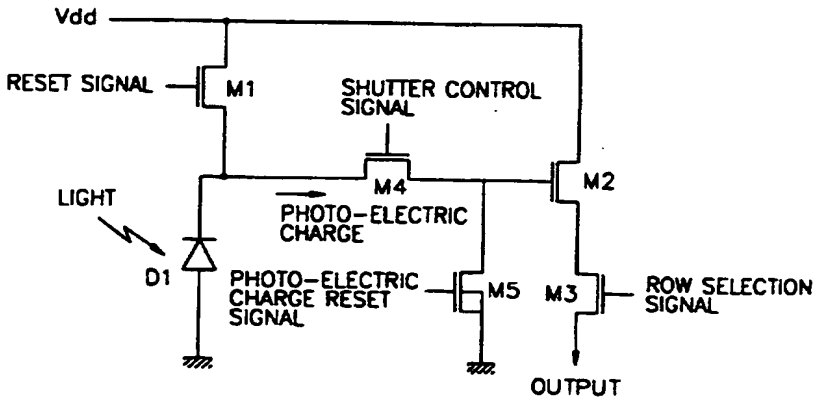

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FIG. 1
CONVENTIONAL ART

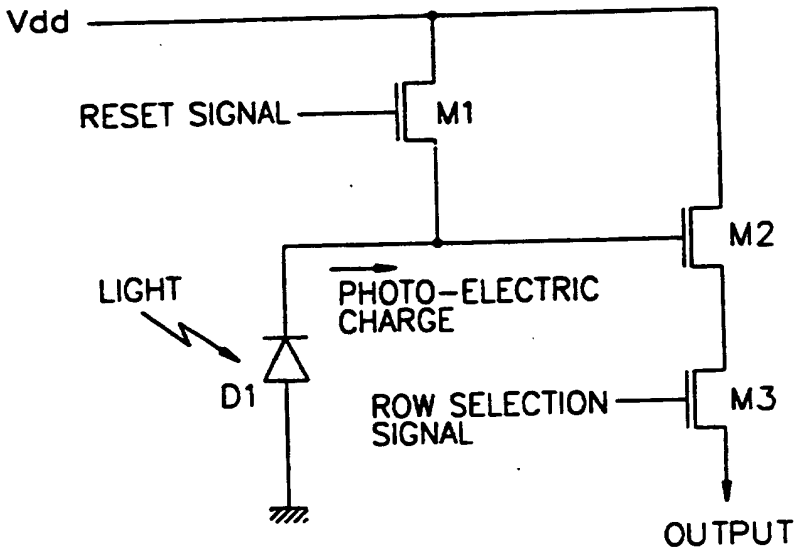


FIG. 2

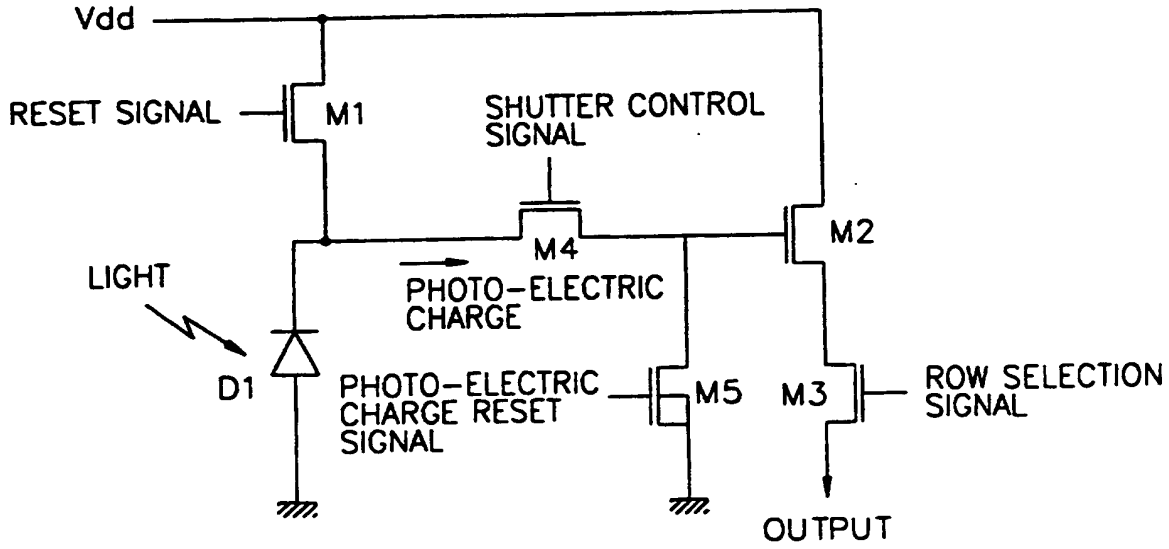


FIG. 3B

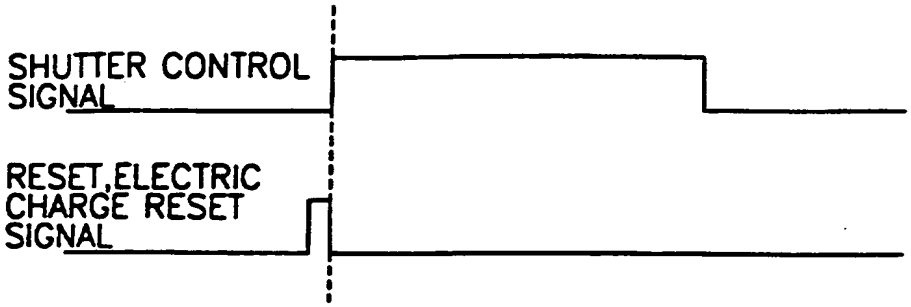


FIG. 3A

FIG. 4A

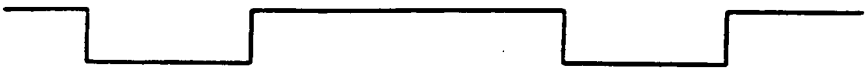


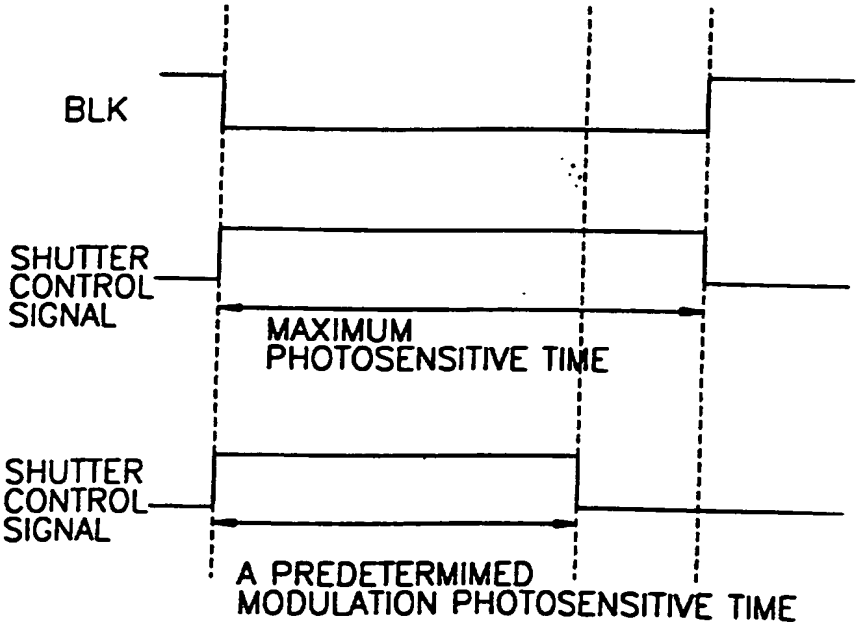
FIG. 4B

FIG. 4C

FIG. 5A

FIG. 5B

FIG. 5C



ACTIVE PIXEL SENSOR WITH ELECTRONIC SHUTTER

The present invention relates to an active pixel sensor (APS) with an electronic shutter, and in particular to an improved active pixel sensor with an electronic shutter that is capable of providing an electronic shutter function as well as an auto exposure function.

Generally, an active pixel sensor (hereinafter called an APS) is formed of two-dimensional sensor arrangements by which an address designation is made possible and has the same RAM construction as the conventional art.

As shown in Figure 1 of the accompanying drawings, the conventional APS includes a photo-diode D1 connected to a ground and generating a photo-electric charge based on externally transmitted light, and three NMOS transistors M1, M2, and M3. The drain of transistor M1 is connected to the photo-diode D1, its source to a power supply rail Vdd, and its gate to a reset signal RESET from a rest signal input for discharging the internal electric charge of the photo-diode D1. The NMOS transistor M2, has its gate connected to the drain of the NMOS transistor M1 to receive the photo-electric charge from the photo-diode D1, and its source connected to the supply rail Vdd, and thus amplifies the electric charges from the photo-diode D1. NMOS transistor M3 has its source connected to the drain of the NMOS transistor M2, and its gate connected to receive an externally inputted row selection signal, thereby to generate an output signal containing pixel data in accordance with the row selection signal.

The reset signal RESET is fed from an external signal source into all pixels, respectively, in order to discharge each electric charge from the photo-cells(photo-diodes), and the row selection signals are sequentially applied from an

externally connected row decoder, thereby selecting each pixel .

The operation of the conventional APS will now be explained with reference to Figure 1.

When a high level reset signal is fed to the gate of the first NMOS transistor M1, the transistor M1 is turned on and the internal electric charge of the photo-diode D1 generated in accordance with externally transmitted light in accordance with the output from the first NMOS transistor M1 is discharged, and the first NMOS transistor M1 is turned off.

Thereafter, the photo-diode D1 receives externally transmitted light for a predetermined photosensitive time and generates a photo electric charge. This photo-electric charge,which may be referred to as an image signal, is applied to the gate of the second NMOS transistor M2, which amplifies the charge(image signal) and feeds the amplified signal to the third NMOS transistor M3. The third NMOS transistor M3 then outputs the amplified signal in accordance with a high level row selection signal applied to its gate. A high level reset signal is applied to the gate of the first NMOS transistor M1, and the resulting output signal from transistor M1 discharges the photo-electric charge generated by the photo-diode D1, so that each pixel is reset to an initial state.

The above-described operations are successively repeated. Therefore, in the conventional APS, a photo-electric charge (image signal) is outputted as pixel data.

In the conventional APS, when the column lines (not shown) of the pixels are selected by an external column decoder (not shown), a photo-electric charge (image signal) generated by externally transmitted light incident on the photo-diode D1 for a predetermined, photosensitive, time is

supplied to an externally connected display apparatus (television or monitor) as data of the pixels.

In the conventional APS, it is possible to control the photosensitive time by generating a reset signal of predetermined frequency before applying a row selection signal . In view of the relevance of the photosensitive time to all the pixels, the above-described control method has a problem in that a desired photosensitive time is obtained with respect to only a predetermined pixel. Therefore, since the pixel data are continuously read and outputted, and the pixels have different photosensitive times, it is very difficult, if not impossible, to ensure that the screen of the display apparatus has a uniform brightness.

Accordingly, it is one object of the present invention to provide an active pixel sensor with an electronic shutter which overcomes, or at least alleviates, the aforementioned problem .

It is another object of the present invention to provide an active pixel sensor with an electronic shutter which is capable of obtaining an auto exposure function so that all pixels have substantially identical photosensitive times by controlling the photo-electric charge which is generated in accordance with light transmitted to a photo-diode.

In accordance with one aspect of the present invention, there is provided an active pixel sensor (APS) comprising: photo-electric charge generating means for generating a photo-electric charge in accordance with light incident thereon; electric charge amplifying and outputting means for amplifying and outputting the photo-electric charge from the photo-electric charge generating means; switching means for passing the photo-electric charge for a predetermined time in accordance with an externally supplied shutter control signal; and electric charge storing means for storing the

photo-electric charge from the switching means for a predetermined time and for supplying the stored photo-electric charge to the electric charge amplifying and outputting means in accordance with an electric charge resetting signal.

Thus, it is possible to provide a display apparatus having a uniform brightness screen by arranging for all the pixels to have substantially identical photosensitive times.

In accordance with a further aspect of the present invention, there is provided an active pixel sensor (APS) comprising: a photo-diode, one side of which is connected to ground, for generating a photo-electric charge in accordance with light incident thereon; a first NMOS transistor, wherein its drain is connected to the other side of the photo-diode, its source receives a power voltage, and its gate receives a reset signal, the first transistor being arranged to discharge an internal electric charge from the photo-diode in accordance with a reset signal; a second NMOS transistor, where its source receives the power voltage, the second transistor being arranged to amplify the photo-electric charge received the gate thereof; a third NMOS transistor, wherein its source is connected to the drain of the second NMOS transistor, its gate receives a row selection signal, the third transistor being arranged to provide as an output the photo-electric charge amplified by the second NMOS transistor in accordance with the row selection signal; a fourth NMOS transistor, wherein its source is connected to the drain of the first NMOS transistor and to said other side of the photo-diode, and its gate is switched by a shutter control signal; and a fifth NMOS transistor, wherein its drain is connected to the drain of the fourth NMOS transistor and to the gate of the second NMOS transistor, its source is connected to ground, and its gate receives an electric charge resetting signal,

the fifth transistor being arranged to store an electric charge supplied from the photo-diode through the fourth NMOS transistor and to output the stored electric charge to the gate of the second NMOS transistor.

In accordance with another aspect of the present invention, there is provided an active pixel sensor comprising: a sensor that generates a charge; a first transistor that discharges the sensor based on a first signal; a second transistor that receives and amplifies the charge from the sensor; a third transistor that outputs the amplified charge from the second transistor in accordance with a second signal; a fourth transistor coupled to the sensor that passes the charge based on a third signal; a fifth transistor that receives a fourth signal and is respectively coupled to the fourth transistor and the second transistor, wherein the fifth transistor receives and stores the charge passed from the sensor through the fourth transistor, and wherein the fifth transistor outputs the stored charge to the second transistor based on the fourth signal.

An active pixel sensor and its method of operation in accordance with the present invention, will now be described, by way of example, with reference to the accompanying drawings, wherein:

Figure 2 is a circuit diagram illustrating the active pixel sensor;

Figure 3A is a wave form diagram of a reset signal and electric charge reset signal in the circuit of Figure 2;

Figure 3B is a wave form diagram of a shutter control signal in the circuit of figure 2;

Figures 4A through 4C are wave form diagrams of television synchronous signals in the circuit according to the present invention, of which:

Figure 4A is a wave form diagram of a blank signal;

Figure 4B is a wave form diagram of a vertical synchronous signal of a television; and

Figure 4C is a wave form diagram of a horizontal synchronous signal of a television; and

Figures 5A through 5C are wave form diagrams of modulated shutter control signals in the circuit of Figure 2, of which:

Figure 5A is a wave form diagram of a blank signal;

Figure 5B is a wave form diagram of a shutter control signal with respect to the maximum photosensitive time; and

Figure 5C is a wave form diagram of a shutter control signal with respect to a predetermined modulation photosensitive time.

As shown in Figure 2, the active pixel sensor includes a photo-diode D1, one side of which is connected to ground, the diode D1 generating a photo-electric charge in accordance with light incident thereon, and five NMOS transistors M1, M2, M3, M4 and M5. The drain of the first NMOS transistor M1 is connected to the other side of the photo-diode D1, its source to a power supply rail Vdd, whilst its gate receives a reset signal RESET, for discharging the internal electric charge of the photo-diode D1. The source of the second NMOS transistor M2 receives the power voltage Vdd for amplifying a photo-electric charge fed to its gate. The source of the third NMOS transistor M3 is connected to the drain of the second NMOS transistor M2, and its gate receives a row selection signal. The output of the transistor M3 comprises the photo-electric charge as

amplified by the second NMOS transistor M2 in accordance with the row selection signal.

The source of the fourth NMOS transistor M4 is connected to the drain of the first NMOS transistor M1 and receives a photo-electric charge from the photo-diode D1. The gate of the transistor M4 is switched in accordance with a shutter control signal. The drain of the fifth NMOS transistor M5 is connected to the drain of the fourth NMOS transistor M4 and to the gate of the second NMOS transistor M2.The source of transistor M5 is connected to ground, and its gate receives an electric charge reset signal CHARGE RESET.The fifth transistor M5 stores the electric charge from the photo-diode D1 received through the fourth NMOS transistor M4 and provides an output to the gate of the second NMOS transistor M2.

The reset signal is fed from an external signal source, so that the electric charges generated by the photo-cells are discharged to all pixels. The row selection signals are sequentially supplied from an externally connected row decoder (not shown), thereby selecting each cell. In addition, the electric-charge reset signal is fed from an externally connected signal source so that the electric charge stored in the fifth NMOS transistor M5 is discharged, and the reset signal is used as an electric charge reset signal.

The operation of the active pixel sensor with an electric shutter will now be described

When the reset signal RESET of Figure 3A is fed into the gate of the first NMOS transistor M1, the first NMOS transistor M1 is turned on. The internal electric charge stored in the photo-diode D1 is discharged in accordance with an output signal from the first NMOS transistor M1, and the first NMOS transistor M1 is turned off. Thus, in the initial stage, the internal electric charge stored in the

photo-diode D1 is discharged, so that the electric charge is stored in the photo-diode D1 for a predetermined photosensitive time.

The high level shutter control signal shown in Figure 3B is applied from an externally connected shutter controller (not shown) to the gate of the fourth NMOS transistor M4, in order to turn on the fourth NMOS transistor M4.

In addition, the photo-electric charge (image signal) generated by the photo-diode D1 in accordance with light incident thereon is stored between the gate and source of the fifth NMOS transistor M5 as received through the fourth NMOS transistor M4 while a shutter control signal maintains a high level. The time during which the shutter control signal maintains a high level becomes a photosensitive time. The fifth NMOS transistor M5 acts as a capacitor.

In addition, the photo-electric charge generated by the photo-diode D1 is stored in the fifth NMOS transistor M5 during the photosensitive time when the shutter control signal is maintained at a high level. When the shutter, which is the fourth NMOS transistor M4, is turned off, namely, when the shutter control signal is at a low level, the photo-electric charge stored in the fifth NMOS transistor M5 is not influenced by the electric charge generated by the photo-diode D1.

Thereafter, the photo-electric charge stored in the fifth NMOS transistor M5 is amplified by the second NMOS transistor M2, and the third NMOS transistor M3, which is turned on in accordance with a row signal from an externally connected row decoder (not shown), feeds the photo-electric charge as amplified by the second NMOS transistor M2 to an externally connected display apparatus (not shown).

The electric charge reset signal CHARGE RESET of Figure 3A is applied to the gate of the fifth NMOS transistor M5, and the internal electric charge of the fifth NMOS transistor M5 is discharged. At this time, the reset signal RESET which is applied to the gate of the first NMOS transistor M1 may be used as the electric charge reset signal CHARGE RESET applied to the gate of the fifth NMOS transistor M5.

The above-described routine during which an output from the APS is due to light incident on the photo-diode D1 for a predetermined photosensitive time is referred to as one period. The on-off time of the shutter is referred to as the photosensitive time of the pixel. In addition, the photo-electric charge generated by each pixel is fed to an externally connected display apparatus such as a television or a monitor (not shown) as an output of each pixel.

In the present invention, during one period for obtaining the outputs of the pixels, all pixels have an identical photosensitive time (exposure time), and the photo-electric charge corresponding to the photosensitive time is stored in the fifth NMOS transistor M5 until each pixel is selected by the externally connected row decoder and column decoder. When each pixel is sequentially selected by the row decoder after each column is selected by the column decoder, the pixel data (photo-electric charge) stored in the fifth NMOS transistor M5 are outputted.

At this time, the photosensitive time (exposure time) is fixed by the shutter control time which is controlled by the externally, connected shutter controller (not shown) connected to the fourth NMOS transistor M4.

That is to say, the photosensitive time is controlled by varying the pulse width of the shutter control signal which is applied to the gate of the fourth NMOS transistor M4 which acts as a shutter so that all pixels have the

identical exposure time(photosensitive time) and are thus identically controlled .

The method of controlling the shutter control signals will now be described.

Figures 4A to 4C illustrate TV synchronous signals. Figure 4A illustrates a vertical blank signal BLK by which a scanning line of TV does not appear, Figure 4B illustrates a vertical synchronous signal VD of TV, and Figure 4C is a horizontal synchronous signal VD of TV.

The externally connected shutter controller (not shown) uses the vertical blank signal BLK shown in Figures 4A and 5A so that the scanning lines of TV do not appear. In the interval in which the vertical blank signal BLK is at a low level, namely in a portion in which the scanning lines do not appear, the shutter control signal, shown in Figures 5B and 5C, which can be modulated, is outputted in accordance with a data signal from an externally connected microcomputer (not shown) while the vertical blank signal BLK is enabled.

The pulse width of the shutter control signal is varied in accordance with the data from the externally connected microcomputer (not shown). The pulse width of the shutter control signal becomes a reference which is used to determine the time for which the photo cells receive light or images. The shutter speed is determined in accordance with the pulse width.

Therefore, the photosensitive time (exposure time) is determined by the time (shutter time) during which the fourth NMOS transistor M4 is turned on/off in accordance with the shutter control signal .

In the present APS , each column is selected by an externally connected column decoder, and each pixel is sequentially selected by an externally connected row decoder, thus outputting pixel data. In addition, in each

pixel, the photo-electric charge generated by the photo diode for a predetermined photosensitive time is stored in the fifth NMOS transistor and then outputted therefrom. In this way, it is possible to obtain a substantially uniform brightness screen.

As described above, the photosensitive time is controlled by a shutter control signal, so that all pixels have substantially identical photosensitive times. Therefore, it is possible to obtain a substantially uniform brightness screen for a TV or monitor. In addition, it is possible to enable a desired auto exposure function for a camera, including a movie digital camera.

Claims

1. An active pixel sensor (APS) comprising:

photo-electric charge generating means for generating a photo-electric charge in accordance with light incident thereon;

electric charge amplifying and outputting means for amplifying and outputting the photo-electric charge from the photo-electric charge generating means;

switching means for passing the photo-electric charge for a predetermined time in accordance with an externally supplied shutter control signal; and

electric charge storing means for storing the photo-electric charge from the switching means for a predetermined time and for supplying the stored photo-electric charge to the electric charge amplifying and outputting means in accordance with an electric charge resetting signal.

2. An active pixel sensor (APS) comprising:

a photo-diode, one side of which is connected to ground, for generating a photo-electric charge in accordance with light incident thereon;

a first NMOS transistor, wherein its drain is connected to the other side of the photo-diode, its source receives a power voltage, and its gate receives a reset signal, the first transistor being arranged to discharge an internal electric charge from the photo-diode in accordance with a reset signal;

a second NMOS transistor, wherein its source receives the power voltage, the second transistor being arranged to amplify the photo-electric charge received at the gate thereof;

a third NMOS transistor, wherein its source is connected to the drain of the second NMOS transistor, and its gate receives a row selection signal, the third transistor being arranged to provide as an output the photo-electric charge amplified by the second NMOS transistor in accordance with the row selection signal;

a fourth NMOS transistor, wherein its source is connected to the drain of the first NMOS transistor and to said other side of the photo-diode, and its gate is switched by a shutter control signal; and

a fifth NMOS transistor, wherein its drain is connected to the drain of the fourth NMOS transistor and to the gate of the second NMOS transistor, its source is connected to ground, and its gate receives an electric charge resetting signal, the fifth transistor being arranged to store an electric charge supplied from the photo-diode through the fourth NMOS transistor and to output the stored electric charge to the gate of the second NMOS transistor.

3. An active pixel sensor according to claim 2, wherein said fourth NMOS transistor is turned on/off in accordance with an externally supplied shutter control signal, thereby operating as an electronic shutter.

4. An active pixel sensor according to claim 3, wherein said shutter control signal is modulated by an externally connected shutter controller in a interval while a vertical blank signal of a TV synchronous signal is at low level, whereby the shutter control signal has a shutter speed corresponding to a data signal from an externally connected microcomputer.

5. An active pixel sensor of according to any one of claims 2 to 4, wherein said fifth NMOS transistor stores only an electric charge generated by the photo diode for a

predetermined photosensitive time during which light is incident thereon.

6. An active pixel sensor according to claim 5, wherein said photosensitive time is determined in relation to the width of a portion of the wave form during which the shutter control signal from the shutter controller is at a high level.

7. An active pixel sensor according to any one of cliams 2 to 6, wherein said reset-signal discharges an electric charge which is generated by the photo-diode, and said electric charge reset signal is supplied for discharging the electric charge stored in the fifth NMOS transistor, and wherein the reset signal is used as an electric charge reset signal.

8. An active pixel sensor comprising:

a sensor that generates a charge;

a first transistor that discharges the sensor based on a first signal;

a second transistor that receives and amplifies the charge from the sensor;

a third transistor that outputs the amplified charge from the second transistor in accordance with a second signal;

a fourth transistor coupled to the sensor that passes the charge based on a third signal;

a fifth transistor that receives a fourth signal and is respectively coupled to the fourth transistor and the second transistor, wherein the fifth transistor receives and stores the charge passed from the sensor through the fourth transistor, and wherein the fifth transistor outputs the

stored charge to the second transistor based on the fourth signal.

9. An active pixel sensor according to claim 8, wherein said fourth transistor operates as an electronic shutter control, and wherein the fourth signal is a shutter control signal that is modulated during a prescribed interval.

10. An active pixel according to claim 8 or claim 9, wherein the sensor is a photo-diode, and wherein said fifth transistor only stores a photo-electric charge generated by light incident on the photo-diode during a photosensitive time based on the third signal.

11. An active pixel sensor according to any one of claims 8 to 10, wherein the first signal discharges the charge generated by the sensor and the fourth signal discharges the stored charge in the fifth transistor, and wherein the first signal is used as the fourth signal.

12. An active pixel sensor according to any one of claims 8 to 11, wherein the second transistor has a first electrode coupled to a second prescribed voltage, and a control electrode coupled to the second electrodes of the fourth and fifth transistors.

13. An active pixel sensor according to any one of claims 8 to 12, wherein the third transistor has a first electrode coupled to a second electrode of the second transistor and a control electrode that receives the second signal.

14. An active pixel sensor according to any one of claims 8 to 13, wherein the fourth transistor has a first electrode coupled to the sensor and the second electrode of the first

transistor, and a control electrode coupled to the third signal.

15. An active pixel sensor according to any one of claims 8 to 14, wherein the fifth transistor has a first electrode coupled to a second electrode of the fourth transistor and a control electrode of the second transistor, a first electrode coupled to a first voltage potential, and a control electrode that receives the fourth signal.

16. An active pixel sensor substantially as hereinbefore described with reference to Figures 2 to 5 of the accompanying drawings.

The Patent Office

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Application No: GB 9820304.5
Claims searched: 1, 2 and 8

Examiner: Bob Clark
Date of search: 29 January 1999

Patents Act 1977
Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.Q): G1A (ASS); H4F (FCCA, FCCE)

Int Cl (Ed.6): H04N 3/15

Other: Online: WPI

Documents considered to be relevant:

Category	Identity of document and relevant passage	Relevant to claims
X	US 5539458 (YAMADA) Column 4 line 62 to column 5 line 54	1

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
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